Preface

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Biographical notes: Mohammad Ayoub Khan is working with the Center for Development of Advanced Computing (Ministry of Communication and IT), India, with interests in radio frequency identification, microcircuit design, and signal processing, NFC, front end VLSI (electronic design automation, circuit optimisation, timing analysis), placement and routing in network-on-chip, etc. He has more than seven years' experience in his research area. He has published more than 50 papers in reputable journals and international IEEE conferences. He contributes to the research community by various voluntary activities. He has served as conference chair in various IEEE/Springer international conferences. He is a member of professional bodies of IEEE, ACM, ISTE and EURASIP society. He is also a member of the technical committees of various journals of IEEE, Springer and Elsevier. Recently, he has also co-authored/edited three books.

Abdul Quaiyum Ansari is working with the Department of Electrical Engineering at Jamia Millia Islamia, New Delhi, India. He received his BTech from AMU, Aligarh, and MTech (IEC) and PhD from IIT Delhi and JMI, New Delhi, respectively. His research is in the areas of computer networks, networks-on-chip, image processing and fuzzy logic. He has published about 100 research papers in international and national journals and proceedings of conferences. He is a Fellow of IETE, and IE(I). He is also presently the Chairman of the Delhi Chapter of the IEEE-Computational Intelligence Society.

Ajith Abraham received his PhD from Monash University, Melbourne, Australia and MSc from Nanyang Technological University, Singapore. His research and development experience includes over 17 years in the industry and academia, spanning different continents in Australia, America, Asia and Europe. He works in a multi-disciplinary environment involving computational intelligence, network security, sensor networks, e-commerce, web intelligence, web services, computational grids, and data mining, and their application to various real world problems. He has authored/co-authored over 800 refereed journal/conference papers and book chapters, and some of the papers have won best paper awards at international conferences and also received several citations. He is a senior member of IEEE, IEEE Computer Society, IEE (UK), ACM, etc.

The increasing demand of numerous applications in consumer electronics has increased the number of computing resources on a single chip. In such a scenario, applications need many computing resources to build a system using system-on-chip (SoC). Therefore, interconnection between each component of SoC becomes another challenging issue. In such a scenario, we need low-power and high-performance systems. Set-top boxes, wireless base stations, HD-TV, mobile phones, and tablets are just a few applications of complex SoC. The applications need many computational resources, such as CPU, multimedia processor, memory cores, and custom

IPs to build a SoC. A conventional approach to SoC applications is to use a shared bus interconnection, which needs arbitration logic to serialise several bus access requests. Many complex SoC solutions have been developed using shared bus mechanism. The bus provides a low-cost solution and simple control characteristics. However, in a bus, only one master at a time can use the bus. Other devices will wait until the bus is free. In such a scenario where the number of bus requests is large and their required bandwidth for interconnection is more than the available bandwidth, interconnections other than a bus should be considered. This has attracted the attention of many researchers towards computer networks. Researchers have started borrowing the concepts of computer networks in SoC design, called emerging trends in on-chip communications or network-on-chip (NoC).

We received several paper submissions for this special issue on NoC, which were all peer-reviewed by 18 professional reviewers. Finally, six submissions were accepted for publication.

The first paper, titled 'A highly efficient behavioural model of router for network-on-chip with link aggregation' proposes a new method of link aggregation (LAG) in NoC. The authors propose a fast SystemC model and its synthesisable System Verilog counterpart for LAG. They also show how the presented model has reduced the simulation time.

The second paper, 'Sphere-based topology for networks-on-chip', proposes a novel sphere-based topology for NoC design, which has less power and delay. The authors have compared the proposed sphere-based topology with existing topologies and have found it to be suitable for NoC applications.

The third paper, 'Acyclic LBDRe: fault-tolerant routing algorithm for network on chip' is also related to the routing algorithm, and proposes a fault-tolerant model for NoC routing. The authors have proposed an acyclic routing algorithm based on an extended logic-based distributed routing (LBDRe) array. The presented algorithm guarantees that not more than one-third of all turns in the NoC architecture become prohibited. The proposed algorithm outperforms substantially the existing fault-tolerant routing algorithms. The authors also show that the proposed method can noticeably reduce the overall average latency and total network power with minimum hardware cost for the fault-tolerant routing algorithm for NoC.

The fourth paper, 'Topologies and routing strategies in MPSoC', presents an investigation of 3D topologies for NoC. The authors argue that current NoCs are implemented predominantly in 2D architectures, which are not area efficient. And, the demand is increasing for more and more area-efficient devices. The authors also show the architectures of the most widely used topologies, such as 3D mesh and torus. They present an algorithm that helps in locating the wrap-around edges in the torus. Finally, a net-list level post layout simulation has been conducted and verified.

The fifth paper, 'Low power clock gating techniques for synchronous buffer-based queue for 3D MPSoC', belongs to the design of virtual channel for NoC. The authors have discussed the role of virtual channels in the design of NoC. The paper presents investigations on existing buffering technique for NoC. Finally, the authors have designed a synchronous queue for 3D NoC that could perform read-and-write operation at the same time. To save power, the authors have presented four different low power techniques to design memory for proposed queue.

The sixth paper, 'Automated transistor width optimisation algorithms for digital circuits', presents an interesting discussion and result for NoC design at transistor level. The authors present a novel automated transistor width optimisation technique based on Levenberg-Marquardt (LM) algorithm (embedded in SPICE) and logical effort theory proposed by Evan Sutherland. They show how these optimisation techniques could be used for designing NoC applications at transistor level, and an efficient integration of TCL and SPICE tool for transistor width optimisation.

We thank the authors who submitted their excellent research works to this special issue titled 'Emerging trends in on-chip communications', and all the reviewers who offered their time and provided numerous useful comments to make the submitted research works much better. Further, this special issue could not have been published without a publisher. We wish to thank the Editor-in-Chief Dr. M.A. Dorgham, Ms. Dana Mitchell, and Mr. Dick Sharp of *International Journal of Embedded Systems* for their efforts and support.